

IN THE CLAIMS

1 1. (Twice Amended) A nonvolatile memory cell array comprised of a plurality of
 2 EEPROM memory cells, each cell comprising:
 3 a semiconductor substrate having a top surface;
 4 a vertical MOS transistor formed by alternating N-type and P-type doped layers
 5 in said substrate and wherein a well is etched into said substrate through said
 6 alternating N-type and P-type layers such that said alternating layer surround said
 7 well, said well having a floating gate of conductive material formed therein which is self
 8 aligned so as to have only components that are orthogonal to said top surface of said
 9 substrate and so as to not extend laterally beyond edges of said well and insulated from
 10 and overlying said alternating N-type and P-type layers by a layer of gate insulating
 11 material;
 12 a word line contact comprising a layer of conductive material formed on said
 13 substrate so as to extend down into said well and overlie said floating gate but insulated
 14 therefrom by an insulation layer; and
 15 a bit line contact comprising a layer of conductive material formed [on] all
 16 portions of which are formed above said top surface of said substrate so as to be in
 17 electrical contact with the drain region of said vertical MOS transistor formed in said
 18 substrate at the location of each vertical MOS transistor in said array.

1 2. (Twice Amended) A nonvolatile memory cell array comprised of a plurality of
 2 nonvolatile memory cells, each memory cell comprising:
 3 a semiconductor substrate having a top surface and having a drain region of a
 4 first conductivity type formed [therein and having a] below said top surface so as to have

5 a surface coincident with said top surface of said substrate and suitable to act as a drain
6 region of a vertical MOS transistor;

7 a buried layer channel region in said semiconductor substrate doped so as to have
8 a second conductivity type having the majority of charge carriers therein of a different
9 polarity than said first conductivity type and suitable to act as a channel of a vertical
10 MOS transistor formed in said substrate;

11 a source region [of] below said top surface of said semiconductor substrate and
12 below said channel region, said source region being doped so as to have said first
13 conductivity type;

14 a recessed gate window in the form of a well etched in said semiconductor
15 substrate through said first layer of insulating material, said well being deep enough to
16 penetrate through said channel region and into said source region such that at least some
17 portion of the side wall or sidewalls of said trench are bordered by said source, drain
18 and channel regions;

19 an insulating layer covering the bottom of said well;

20 a gate insulating layer formed on the sidewall of said well;

21 a self aligned floating gate comprising a conductive material formed within said
22 well on said gate insulating layer so as to only have a conductive component on said
23 sidewall of said well and not on the bottom of said well no portion of said self aligned
24 floating gate extending [not extend] beyond the edges of said well;

25 an insulating layer formed over said self aligned floating gate so as to electrically
26 isolate said floating gate from all surrounding structures, said floating gate having a
27 dimension suitable so as to overlie at least said channel region;

28 a word line comprising conductive material deposited so as to extend into said

29 well far enough to overlie at least a portion of said floating gate; and
30 a second layer of insulating material formed so as to [insulate at least a portion
31 of] completely cover said word line; and
32 a bit line all portions of which are formed [over] above said top surface of said
33 semiconductor substrate so as to make contact with at least a portion of said drain region
34 at each said memory cell but insulated from said word line by said second layer of
35 insulating material.

1 3. (Amended) A nonvolatile memory cell array comprised of a plurality of EEPROM
2 memory cells, each cell comprising:
3 a semiconductor substrate having a top surface;
4 a vertical MOS transistor formed by a first three-dimensional layer of N-type
5 conductivity [and having] formed within said substrate so as to have a surface coincident
6 with [the] said top surface of said substrate and forming a drain region of said vertical
7 MOS transistor, a second layer of P-type conductivity within said substrate and adjacent
8 to and underlying said first layer relative to [the] said top surface of said substrate and
9 forming a channel region of said vertical MOS transistor, and a third layer of N-type
10 conductivity within said substrate and adjacent to and underlying said second layer and
11 forming a source region of said vertical MOS transistor, and having a well etched into
12 said substrate so as to penetrate through said first and second layers and at least
13 partially through said third layer, said well having a floating gate of conductive material
14 formed therein which is self aligned so as to not extend laterally beyond edges of said
15 well and so as to have only a conductive component on the walls of said well but not on the
16 bottom thereof. [and] said self aligned floating gate overlying said first, second and third